MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Order this document
by MC88110EC/D

MC88110

Advance Information

MC88110 RISC Microprocessor

This document contains electrical characteristics, pin grid array pinouts, and mechanical drawings for the MC88110. It is divided into three distinct sections: MC88110 Preliminary Electrical Specifications, MC88110 Pin Grid Array Pinout, and MC88110 Mechanical Drawing. The contents of this document are arranged as follows:

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC88110 Preliminary Electrical Specifications

***WARNING**: The following electrical and timing specifications are preliminary and subject to change without notice. These figures are approximate, use them for tentative planning purposes only.*

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{dd}	-0.3 to +7.0	V
Input Voltage	V_{in}	-0.8 to +7.0	V
Maximum Operating Junction Temperature	T_J	110	°C
Recommended Operating Junction Temperature Range	T_J	0 to 85	°C
Storage Temperature Range	T_{stg}	-55 to 150	°C

Table 2. DC Electrical Characteristics

Characteristic	Comments	Symbol	Min	Max	Unit
Input High Voltage	All inputs except the CLK	V_{IH}	2	V_{dd}	V
Input Low Voltage	All inputs except the CLK	V_{IL}	GND	0.8	V
CLK Input High Voltage		CV_{IH}	2.4	V_{dd}	V
CLK Input Low Voltage		CV_{IL}	GND	0.5	V
Input Leakage Current $GND<=V_{IN}<=V_{dd}$		I_{in}	TBD	TBD	µa
Hi-Z (Off-State) Leakage Current @ 0.5/2.4 V		I_{TSI}	TBD	TBD	µa
Signal Low Input Current V_{IL}=0.8 V and V_{IH}=2.0 V	TMS,TDI,$\overline{TRST}$	I_{IL}, I_{IH}	50	500	µa
Output High Voltage I_{OH}=20ma		V_{OH}	2.4	–	V
Output Low Voltage I_{OL}=20ma		V_{OL}	–	0.5	V
Capacitance (see Note) V_{in}=0 V, f=1 MHz		C_{in}	–	15	pF
Typical Power Dissipation (ambient)	50 MHz 40 MHz	P_D	– –	10 8.5	W W

NOTE: Capacitance is periodically sampled rather than 100% tested.

Table 3. Clock AC Timing Specifications

V_{dd}=5.0, V_{dc} ± 5%, GND=0 V_{dc}

Num.	Note	Characteristic	40 MHz		50 MHz		Unit
			Min	Max	Min	Max	
		Frequency of Operation	33	40	33	50	MHz
1		CLK Cycle Time	25	30	20	30	ns
2	1	CLK Rise Time	–	2	–	2	ns
3	1	CLK Fall Time	–	2	–	2	ns
4		CLK Duty Cycle Measured at 1.4 V	40	60	40	60	%
4a		CLK Pulse Width High Measured at 1.4 V	10	22	8	22	ns
4b		CLK Pulse Width Low Measured at 1.4 V	10	22	8	22	ns

NOTE: While the rise and fall times for the CLK input will be measured from 0.8 to 2.0 volts, the CLK signal is expected to swing from 0.5 to 2.4 volts.

Table 4. Input AC Timing Specifications

V_{dd}=5.0, V_{dc} ± 5%, GND=0 V_{dc}

Num.	Notes 1, 3	Characteristic	40 MHz		50 MHz		Unit
			Min	Max	Min	Max	
5		Data, Byte Parity in Valid to CLK (setup)	9	–	9	–	ns
6		CLK to Data, Byte Parity in Invalid (hold)	4	–	-3	–	ns
7		$\overline{PTA}$,$\overline{TA}$,$\overline{TEA}$,$\overline{TRTRY}$,$\overline{AACK}$ Valid to CLK (setup)	12	–	9	–	ns
7A		$\overline{ARTRY}$, $\overline{SHD}$ Valid to CLK (setup)	12	–	8	–	ns
8		CLK to $\overline{PTA}$,$\overline{TA}$,$\overline{TEA}$,$\overline{TRTRY}$,$\overline{AACK}$, $\overline{ARTRY}$, $\overline{SHD}$ in Invalid (hold)	-4	–	-3	–	ns
9		$\overline{DBG}$ and $\overline{BG}$ Valid to CLK (setup)	12	–	9	–	ns
10		CLK to $\overline{DBG}$ and $\overline{BG}$ Invalid (hold)	-2	–	-1	–	ns
11	4	Address Valid to CLK (setup)	6	–	4	–	ns
12	4	CLK to Address Invalid (hold)	2	–	2	–	ns
13		$\overline{SR}$ in Valid to CLK (setup)	12	–	9	–	ns
14		CLK to $\overline{SR}$ in Invalid (hold)	-2	–	-1	–	ns
15		$\overline{ABB}$ and $\overline{DBB}$ in Valid to CLK (setup)	12	–	9	–	ns
16		CLK to $\overline{ABB}$ and $\overline{DBB}$ in Invalid (hold)	-2	–	-1	–	ns
17	2	$\overline{NMI}$,$\overline{INT}$,$\overline{RST}$ and $\overline{DBUG}$ Valid to CLK (setup)	6	–	4	–	ns
18		CLK to $\overline{NMI}$,$\overline{INT}$,$\overline{RST}$ and $\overline{DBUG}$ Invalid (hold)	2	–	2	–	ns

NOTES:

1. All input specs are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the input CLK. Input timings are measured at the pin.
2. These signals will pass through one clock of debounce circuitry internal to the processor before being functionally recognized. They need to be held asserted for at least the full span of one clock cycle.
3. These numbers are for operation at the frequency specified in the column heading only.
   For reduced frequency operation of a 50 MHz part apply the following formulas to these specs:
   #5,7,9,13,15: Min = $T_{cyc}/4$ + 4 ns
   #6,8: Min = $-T_{cyc}/4$ + 2 ns
   #7A: Min = $T_{cyc}/4$ + 3 ns
   #10,14,16: Min = $-T_{cyc}/4$ + 4 ns
   For reduced frequency operation of a 40 MHz part apply the following formulas to these specs:
   #5,7,7A,9,13,15: Min = $T_{cyc}/4$ + 5.75 ns
   #6,8: Min = $-T_{cyc}/4$ + 2.25 ns
   #10,14,16: Min = $-T_{cyc}/4.25$ + 4 ns
4. These control signals have timing that coincides with address: $\overline{TBST}$,R/$\overline{W}$,$\overline{INV}$,$\overline{GBL}$.

Table 5. Output AC Timing Specifications

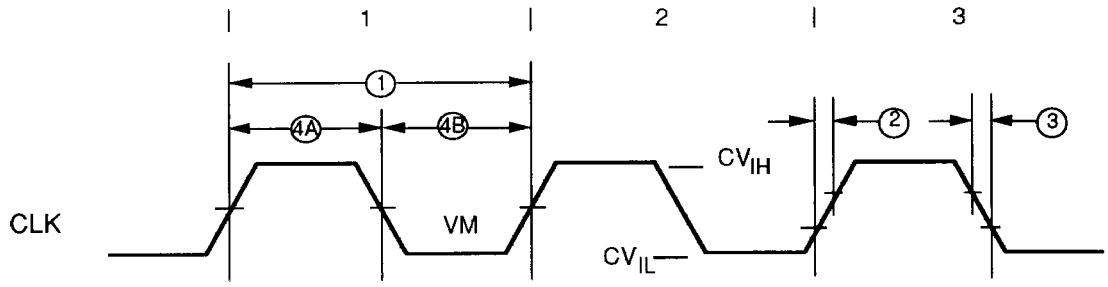
V_{dd}=5.0, V_{dc} ± 5%, GND=0 V_{dc}

Num.	Notes 1,5	Characteristic	40 MHz		50 MHz		Unit
			Min	Max	Min	Max	
19	4	CLK to Address Valid	5	17	4	15	ns
20	4	CLK to Address Invalid	5	–	4	–	ns
21	2	CLK to $\overline{TS}$,$\overline{ABB}$,$\overline{DBB}$ Asserted, Negated	0	11	0	10	ns
22		CLK to Data, Byte Parity, $\overline{BPE}$ out Valid	5	17	4	15	ns
23		CLK to Data,Byte Parity, $\overline{BPE}$ out Invalid	5	–	4	–	ns
24		CLK to Data, Byte Parity, $\overline{BPE}$ out Hi-Impedance	5	15	4	12	ns
25	4	CLK to Address Hi-Impedance	5	15	4	12	ns
26		CLK to $\overline{TS}$,$\overline{ABB}$,$\overline{DBB}$ Hi-Impedance	11	20	9	17	ns
27		CLK to Output Lo-Impedance	5	–	4	–	ns
27A		CLK to $\overline{ABB}$, $\overline{DBB}$, $\overline{TS}$ Lo-Impedance	0	–	0	–	ns
28		CLK to $\overline{BR}$ Asserted	0	11	0	10	ns
29		CLK to $\overline{BR}$ Negated	0	11	0	10	ns
30		CLK to $\overline{SSTAT1}$ and $\overline{SSTAT0}$ Asserted	0	11	0	10	ns
31	3	CLK to $\overline{SSTAT0}$ and $\overline{SSTAT1}$ Negated	–	17	–	15	ns
32		CLK to $\overline{SSTAT0}$ and $\overline{SSTAT1}$ Hi-Impedance	[illegible]	27	14	22	ns
33		CLK to PSTAT2–0 Valid		17	4	15	ns
33A		CLK to PSTAT2–0 Invalid	5	–	4	-	ns

NOTES:

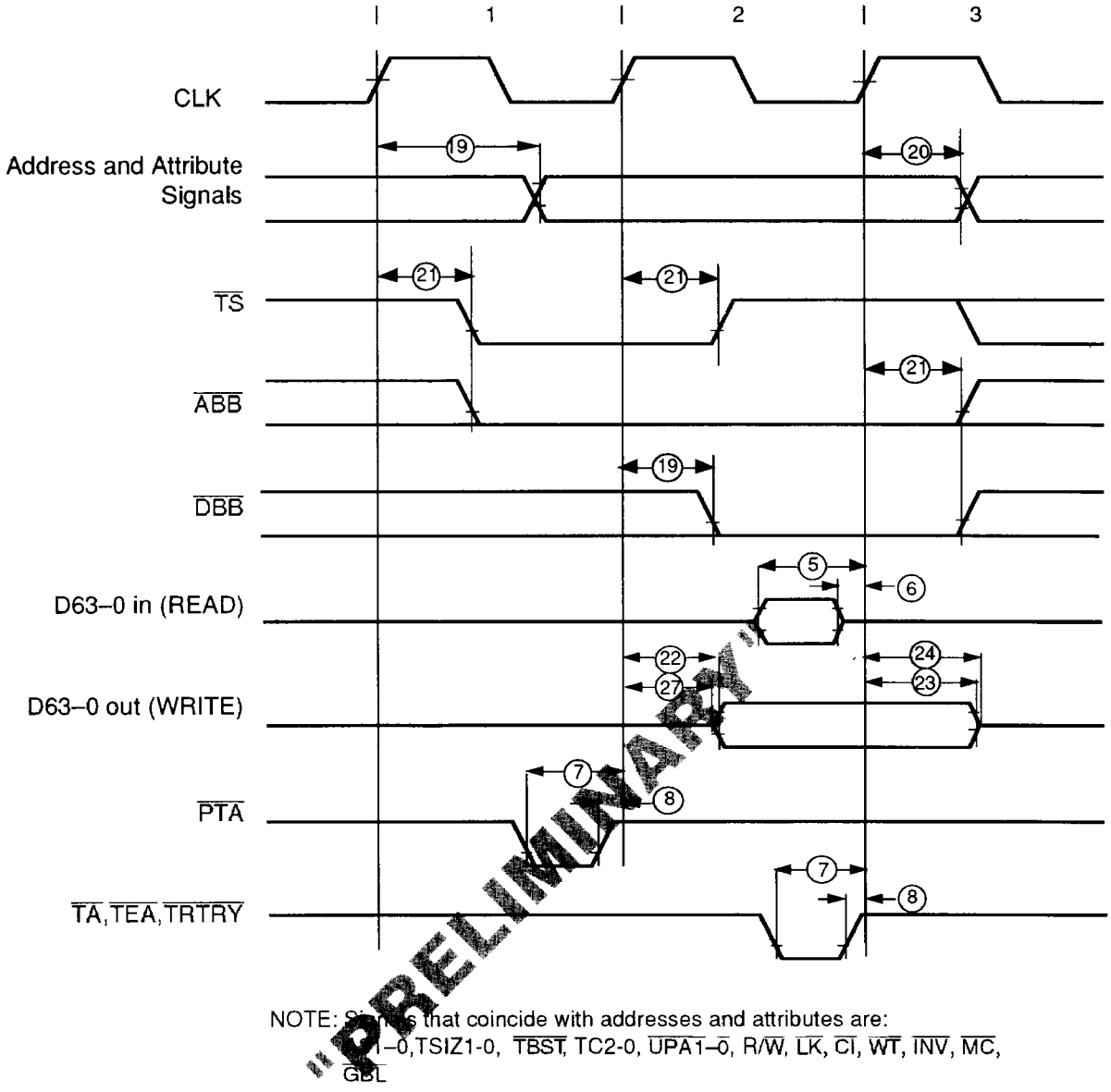
1. All outputs except $\overline{TS}$ and $\overline{SSTAT}$(1–0) are specified with an output load of 50pF and a line length of 6 inches. $\overline{TS}$ and $\overline{SSTAT}$(1–0) are specified with a load of 60pF and a line length of 6 inches. All output timing specifications assume a board impedance in the range of 50 ohms to 90 ohms and a dielectric constant in the range of 2 to 6. All output specs are measured from the 1.4 V of the input CLK to the TTL level (0.8 or 2.0 V) of the signal in question. Outputs are measured both at the pin and at the end of the 6 inch line.
2. The shared outputs $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{SSTAT}$(1–0) must have pull-up resistors to hold them negated when there is no bus master.
3. Because $\overline{SSTAT0}$ and $\overline{SSTAT1}$ may be asserted by more than one processor, they are negated in a unique fashion. First all processors will three-state for 4 ns, and then, the signal will be driven high by all processors. This protocol should prevent driver contention on these signals.
4. These control signals have timing that coincides with address: TSIZ1–0,$\overline{TBST}$,TC3–0, $\overline{UPA1–0}$, R/$\overline{W}$, $\overline{LK}$, $\overline{CI}$, $\overline{WT}$, $\overline{INV}$, $\overline{MC}$, $\overline{GBL}$. $\overline{TS}$, $\overline{ABB}$ and $\overline{DBB}$ are asserted $T_{cyc}/4$ prior to Address.
5. These numbers are for operation at the frequency specified in the column heading only.
   For reduced frequency operation of a 50-MHz part apply the following formulas to these specs:
   - #19,20,22,23,24,25,27,33,33A: Min = $T_{cyc}/4$ -1 ns
   - #19,22,31,33: Max = $T_{cyc}/4$ + 10 ns
   - #24,25: Max = $T_{cyc}/4$ + 7 ns
   - #26: Min = $T_{cyc}/2$ - 1 ns
   - #26: Max = $T_{cyc}/2$ + 7 ns
   - #32: Min = $3T_{cyc}/4$ - 1 ns
   - #32: Max = $3T_{cyc}/4$ + 7 ns

   For reduced frequency operation of a 40-MHz part apply the following formulas to these specs:
   - #19,20,22,23,24,25,27,33,33A: Min = $T_{cyc}/4$ -1.25 ns
   - #19,22,31,33: Max = $T_{cyc}/4$ + 10.75 ns
   - #24,25: Max = $T_{cyc}/4$ + 8.75 ns
   - #26: Min = $T_{cyc}/2$ - 1.5 ns
   - #26: Max = $T_{cyc}/2$ + 8.5 ns
   - #32: Min = $3T_{cyc}/4$ - 1.75 ns
   - #32: Max = $3T_{cyc}/4$ + 8.25 ns



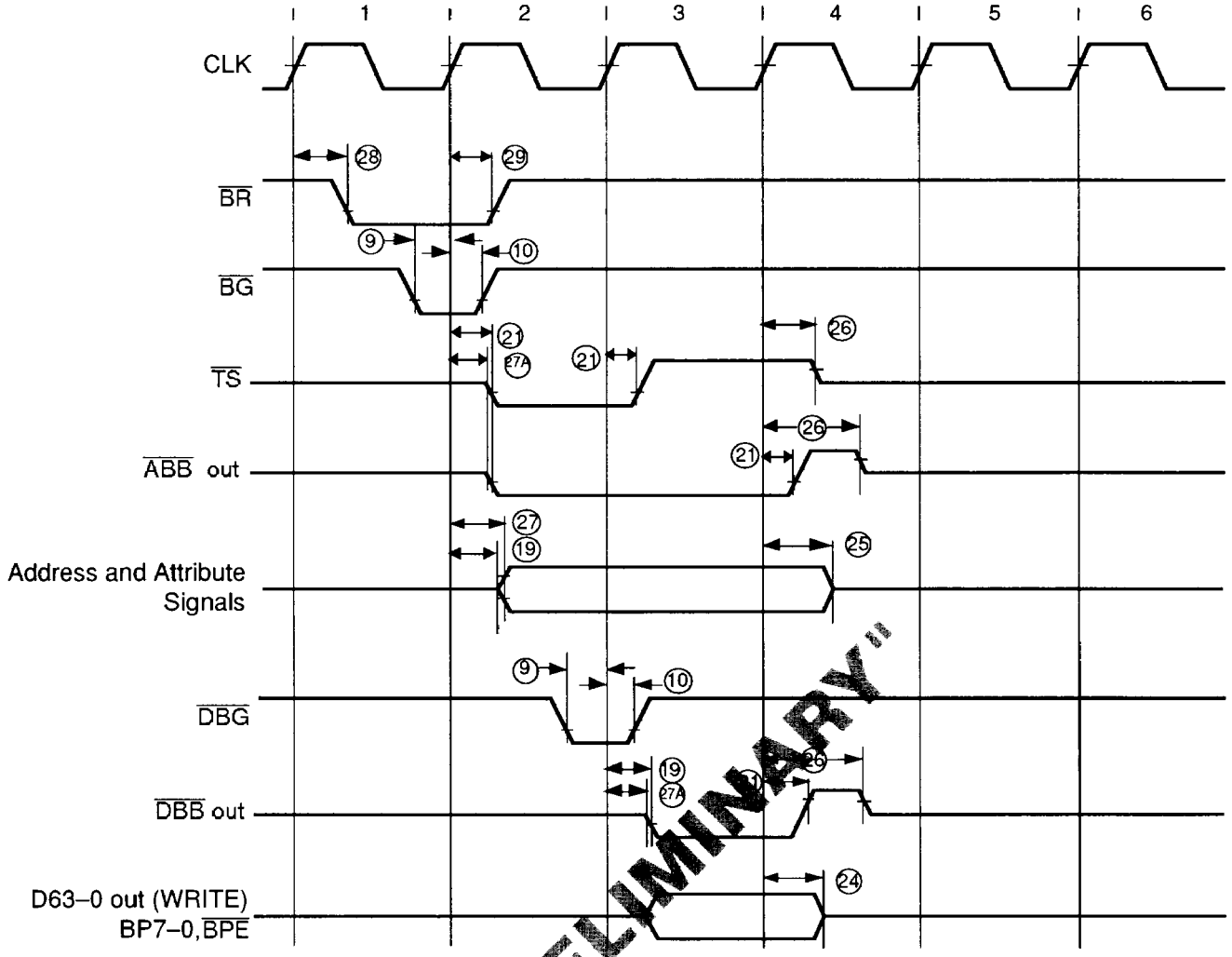
VM = Midpoint Voltage (1.4 V)

Figure 1. Clock Input Timing Diagram



NOTE: Signals that coincide with addresses and attributes are:
A31–0, TSIZ1-0, TBST, TC2-0, UPA1–0, R/W, LK, CI, WT, INV, MC, GBL

Figure 2. Read/Write Timing Diagram



NOTE: Signals that coincide with addresses and attributes are:
A31–0, TT1-0, TBST, TC2-0, UPA1-0, R/W, LK, CI, WT, INV, MC, GBL

Figure 3. Bus Arbitration Timing Diagram

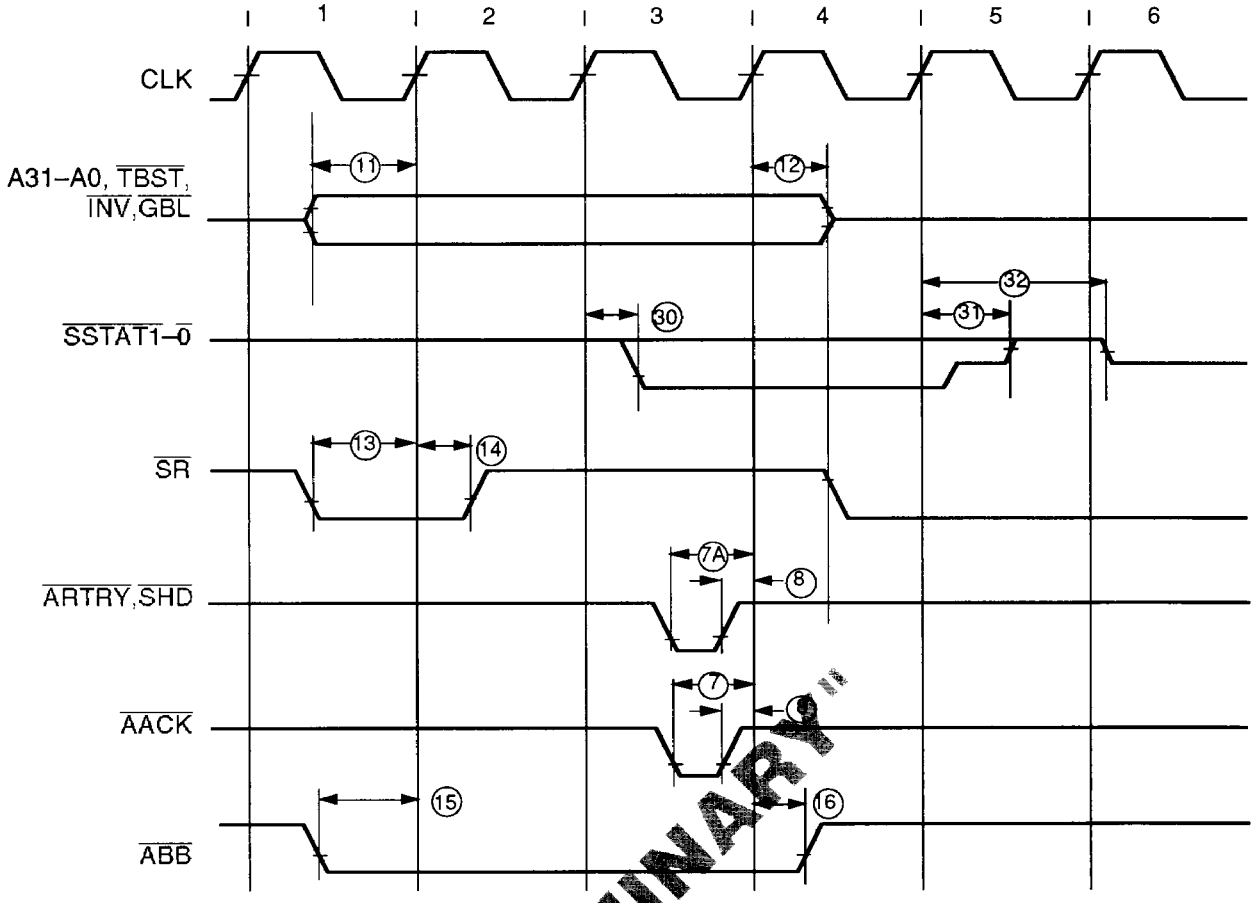


Figure 4. Snoop Timing Diagram

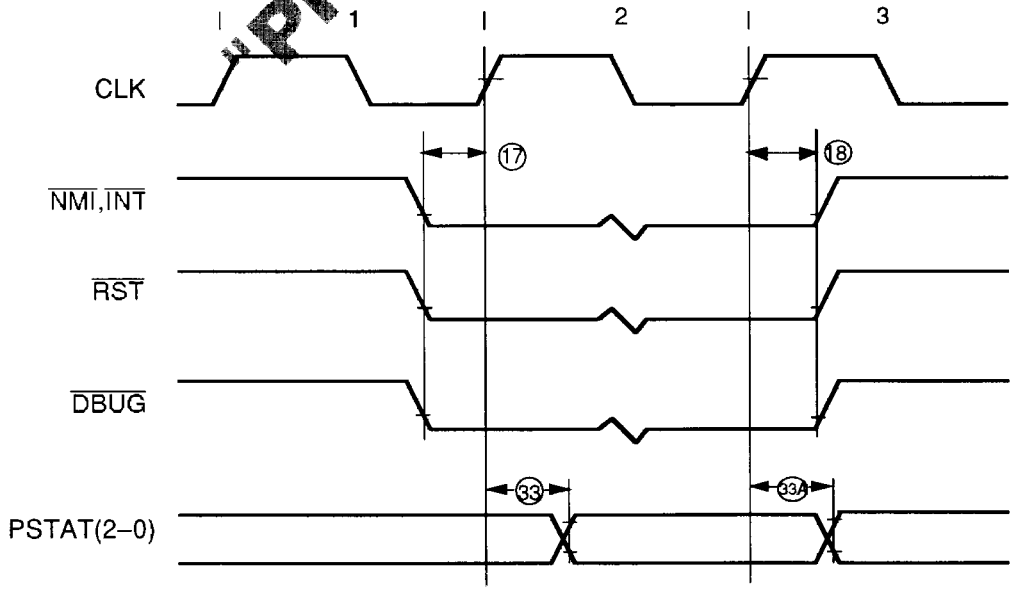


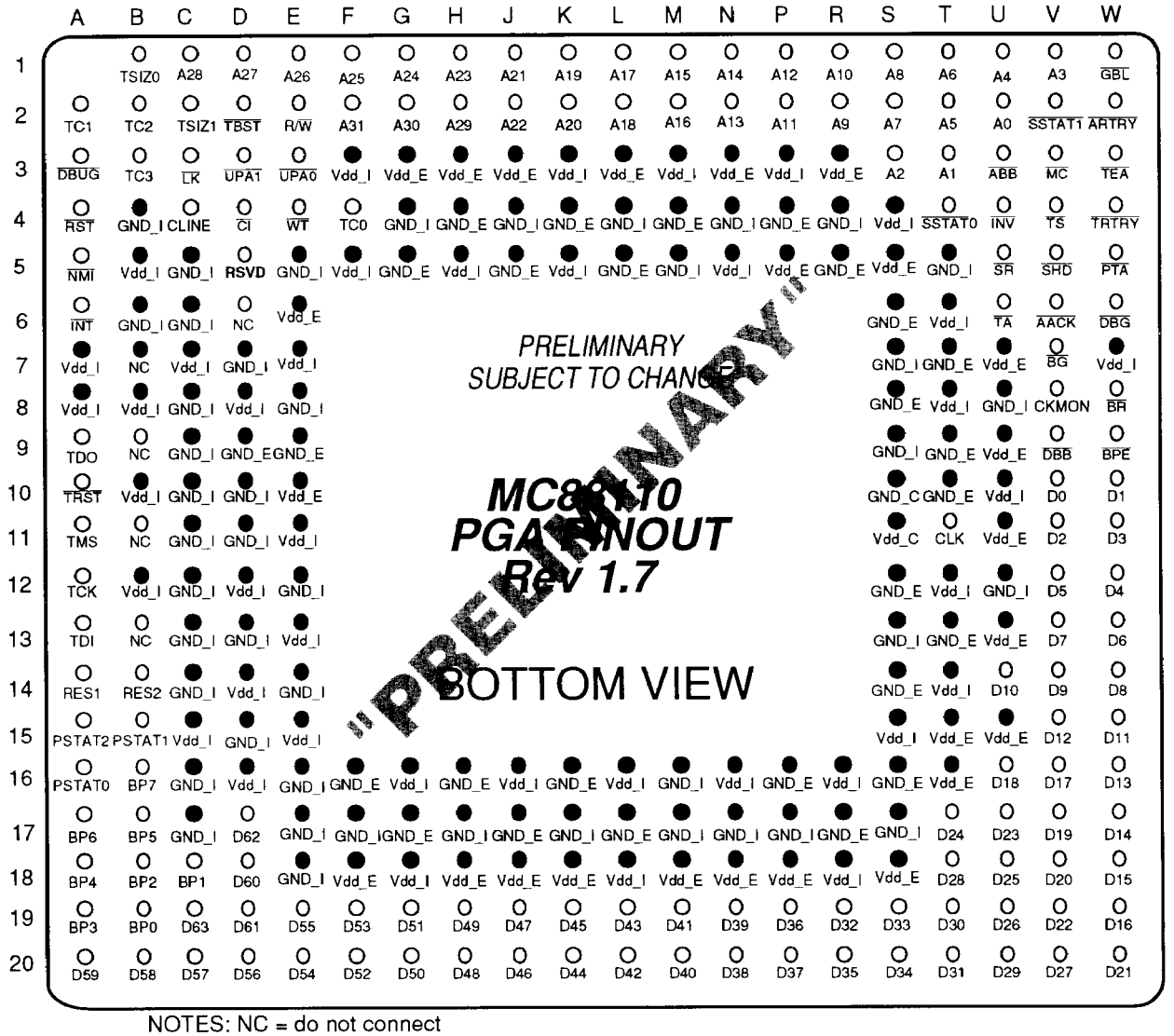
Figure 5. Other Signals Timing Diagram

MC88110 Pin Grid Array Pinout

This section contains the pin assignments and package dimension diagrams for the MC88110, and also information to be used as a guide when ordering.

Pin Assignments

The MC88110 is available in a 299-pin package. The following figure shows the pin assignment for the MC88110. Power and ground pins are divided into those used for internal signals, external signals and buses, and clocking. These groupings are listed in Table 6.



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	V	W
1		TSIZ0	A28	A27	A26	A25	A24	A23	A21	A19	A17	A15	A14	A12	A10	A8	A6	A4	A3	$\overline{GBL}$
2	TC1	TC2	TSIZ1	$\overline{TBST}$	R/$\overline{W}$	A31	A30	A29	A22	A20	A18	A16	A13	A11	A9	A7	A5	A0	$\overline{SSTAT1}$	$\overline{ARTRY}$
3	$\overline{DBUG}$	TC3	$\overline{LK}$	$\overline{UPA1}$	$\overline{UPA0}$	Vdd_I	Vdd_E	Vdd_E	Vdd_E	Vdd_I	Vdd_E	Vdd_I	Vdd_E	Vdd_I	Vdd_E	A2	A1	$\overline{ABB}$	$\overline{MC}$	$\overline{TEA}$
4	$\overline{RST}$	GND_I	CLINE	$\overline{CI}$	$\overline{WT}$	TC0	GND_I	GND_E	GND_I	GND_E	GND_I	GND_E	GND_I	GND_E	GND_I	Vdd_I	$\overline{SSTAT0}$	$\overline{INV}$	$\overline{TS}$	$\overline{TRTRY}$
5	$\overline{NMI}$	Vdd_I	GND_I	**RSVD**	GND_I	Vdd_I	GND_E	Vdd_I	GND_E	Vdd_I	GND_E	GND_I	Vdd_I	Vdd_E	GND_E	Vdd_E	GND_I	$\overline{SR}$	$\overline{SHD}$	$\overline{PTA}$
6	$\overline{INT}$	GND_I	GND_I	NC	Vdd_E											GND_E	Vdd_I	$\overline{TA}$	$\overline{AACK}$	$\overline{DBG}$
7	Vdd_I	NC	Vdd_I	GND_I	Vdd_I											GND_I	GND_E	Vdd_E	$\overline{BG}$	Vdd_I
8	Vdd_I	Vdd_I	GND_I	Vdd_I	GND_I											GND_E	Vdd_I	GND_I	CKMON	$\overline{BR}$
9	TDO	NC	GND_I	GND_E	GND_E											GND_I	GND_E	Vdd_E	$\overline{DBB}$	$\overline{BPE}$
10	$\overline{TRST}$	Vdd_I	GND_I	GND_I	Vdd_E											GND_C	GND_E	Vdd_I	D0	D1
11	TMS	NC	GND_I	GND_I	Vdd_I											Vdd_C	CLK	Vdd_E	D2	D3
12	TCK	Vdd_I	GND_I	Vdd_I	GND_I											GND_E	Vdd_I	GND_I	D5	D4
13	TDI	NC	GND_I	GND_I	Vdd_I											GND_I	GND_E	Vdd_E	D7	D6
14	RES1	RES2	GND_I	Vdd_I	GND_I											GND_E	Vdd_I	D10	D9	D8
15	PSTAT2	PSTAT1	Vdd_I	GND_I	Vdd_I											Vdd_I	Vdd_E	Vdd_E	D12	D11
16	PSTAT0	BP7	GND_I	Vdd_I	GND_I	GND_E	Vdd_I	GND_E	Vdd_I	GND_E	Vdd_I	GND_I	Vdd_I	GND_E	Vdd_I	GND_E	Vdd_E	D18	D17	D13
17	BP6	BP5	GND_I	D62	GND_I	GND_I	GND_E	GND_I	GND_E	GND_I	GND_E	GND_I	GND_I	GND_I	GND_E	GND_I	D24	D23	D19	D14
18	BP4	BP2	BP1	D60	GND_I	Vdd_E	Vdd_I	Vdd_E	Vdd_E	Vdd_E	Vdd_I	Vdd_E	Vdd_E	Vdd_E	Vdd_I	Vdd_E	D28	D25	D20	D15
19	BP3	BP0	D63	D61	D55	D53	D51	D49	D47	D45	D43	D41	D39	D36	D32	D33	D30	D26	D22	D16
20	D59	D58	D57	D56	D54	D52	D50	D48	D46	D44	D42	D40	D38	D37	D35	D34	D31	D29	D27	D21

NOTES: NC = do not connect
CKMON is an output test pin and should be left unconnected
RSVD should be pulled to Vdd through a 10K ohm resistor

Table 6. MC88110 Signals and Pin Locations

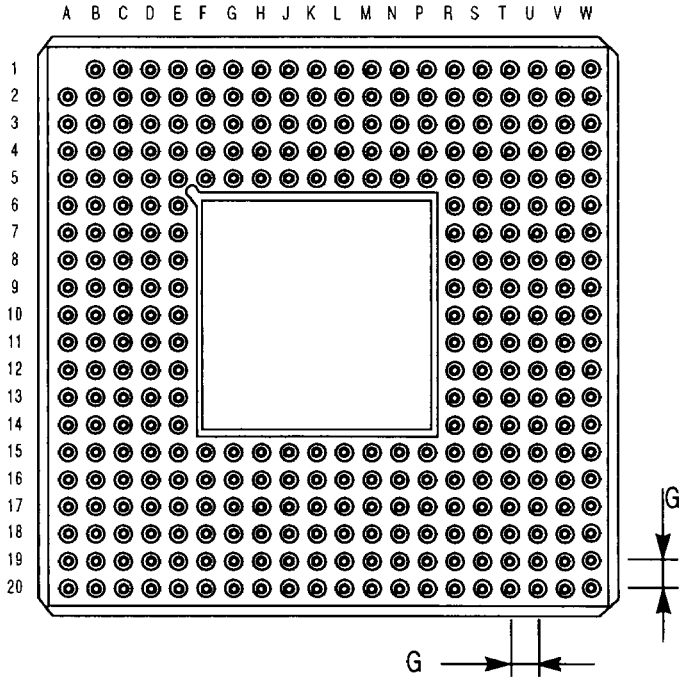
Signal	Pin Location
Internal Logic V_{dd}	A7, A8, B5, B8, B10, B12, C7, C15, D8, D12, D14, D16, E7, E11, E13, E15, F3, F5, G16, G18, H5, J16, K3, K5, L16, L18, M3, N5, N16, P3, R16, R18, S4, S15, T6, T8, T12, T14, U10, W7
External Signals and Buses V_{dd}	E6, E10, F18, G3, H3, H18, J3, J18, K18, L3, M18, N3, N18, P5, P18, R3, S5, S18, T16, U7, U9, U11, U13, U15, T15
Clock Vdd	S11
Internal Logic GND	B4, B6, C5, C6, C8, C9, C10, C11, C12, C13, C14, C16, C17, D7, D10, D11, D13, D15, E5, E8, E12, E14, E16, E17, E18, F17, G4, H17, J4, K17, L4, M5, M16, M17, N4, N17, P17, R4, S7, S9, S13, S17, T5, U8, U12
External Signals and Buses GND	D9, E9, F16, G5, G17, H4, H16, J5, J17, K4, K16, L5, L17, M4, P4, P16, R5, R17, S6, S8, S12, S14, S16, T7, T9, T10, T13
Clock GND	S10
CLK	T11
A31–0	F2,G2,H2,C1,D1,E1,F1,G1,H1,J2,J1,K2,K1,L2,L1,M2,M1,N1,N2,P1,P2, R1,R2,S1,S2,T1,T2,U1,V1,S3,T3,U2
$\overline{TS}$	V4
TSIZ1–0	C2,B1
R/$\overline{W}$	E2
TC3–0	B3,B2,A2,F4
$\overline{LK}$	C3
$\overline{WT}$	E4
$\overline{UPA1–0}$	D3,E3
$\overline{CI}$	D4
$\overline{MC}$	V3
$\overline{INV}$	U4
$\overline{GBL}$	[illegible]
$\overline{TBST}$	D2
CLINE	C4
PSTAT2–0	A15,B15,A16
D63–0	C19,D17,D19,D18,A20,B20,C20,D20,E19,E20,F19,F20,G19,G20,H19,H20,J19,J20,K19,K20,L19,L20,M19,M20,N19,N20,P20,P19,R20,S20,S19,R19,T20,T19,U20,T18,V20,U19,U18,T17,U17,V19,W20,V18,V17,U16,V16,W19,W18,W17,W16,V15,W15,U14,V14,W14,V13,W13,V12,W12,W11,V11,W10,V10
BP7–0	B16,A17,B17,A18,A19,B18,C18,B19
$\overline{TA}$	U6
$\overline{TEA}$	W3
$\overline{TRTRY}$	W4
$\overline{PTA}$	W5
$\overline{SR}$	U5
$\overline{SSTAT1–0}$	V2,T4
$\overline{ARTRY}$	W2
$\overline{SHD}$	V5
$\overline{AACK}$	V6

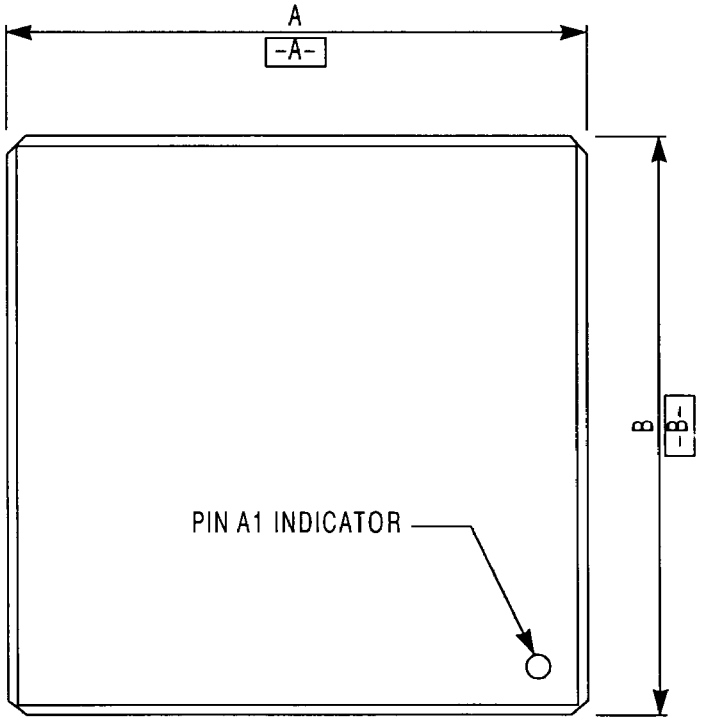
Table 6. MC88110 Signals and Pin Locations (concluded)

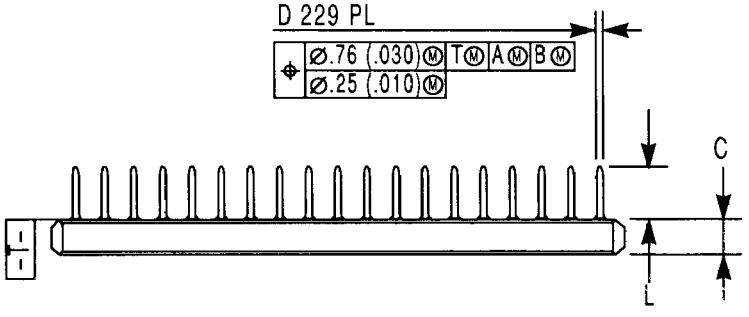
Signal	Pin Location
$\overline{BG}$	V7
$\overline{BR}$	W8
$\overline{ABB}$	U3
$\overline{DBG}$	W6
$\overline{DBB}$	V9
$\overline{DBUG}$	A3
$\overline{BPE}$	W9
$\overline{NMI}$	A5
$\overline{INT}$	A6
$\overline{RST}$	A4
TDI	A13
TMS	A11
$\overline{TRST}$	A10
TCK	A12
TDO	A9
RES2	B14
RES1	A14
RSVD	D5
CKMON	V8
NC	B7,B9,B11,B13,B6

MC88110 Mechanical Drawing

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: Inch







Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	51.82	52.83	2.040	2.080
B	51.82	52.83	2.040	2.080
C	2.80	3.55	0.110	0.140
D	0.43	0.48	0.017	0.019
G	2.54	BSC	0.100	BSC
L	3.81	4.31	0.150	0.170