

BugLabs Module Design Handbook
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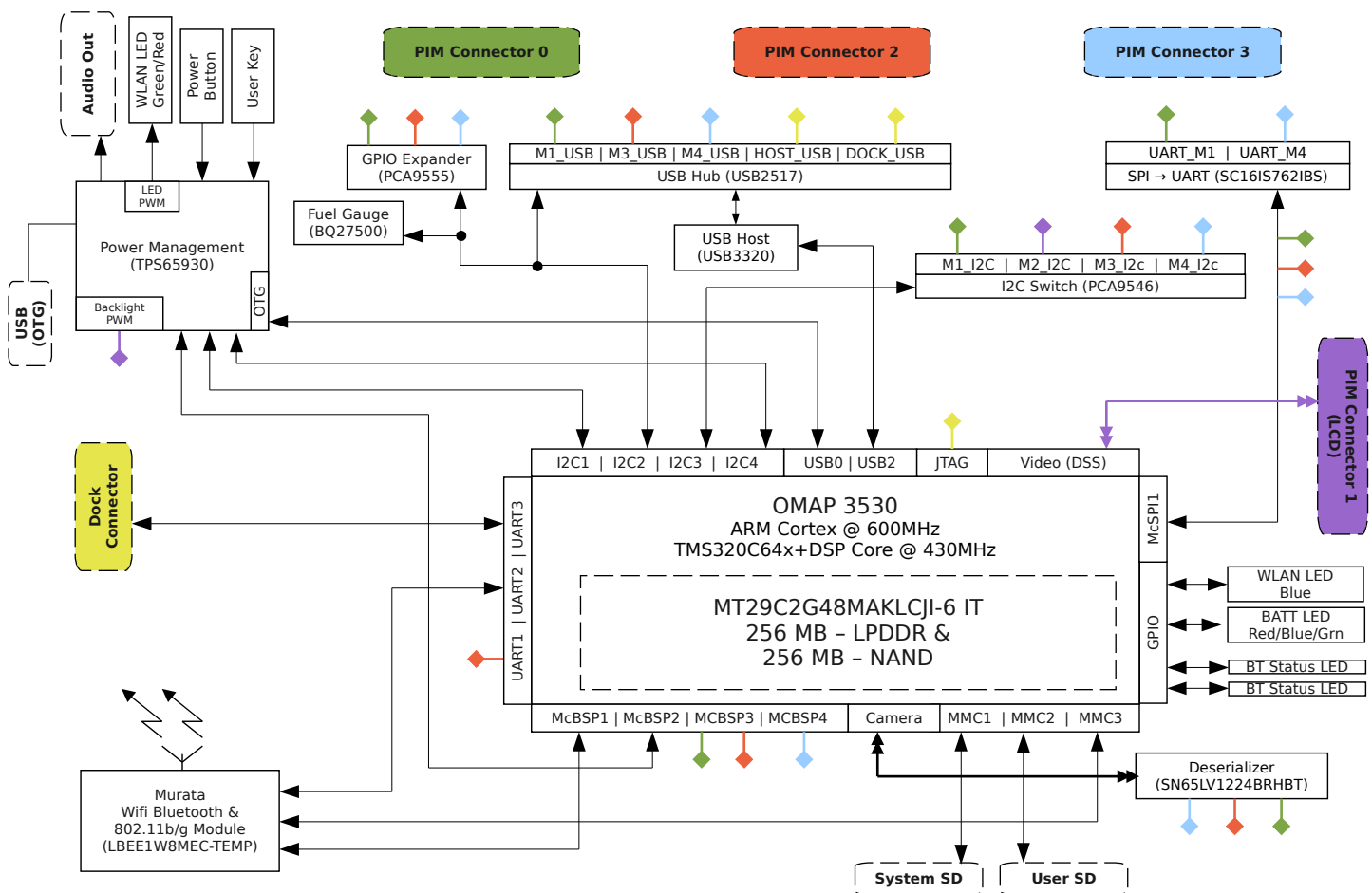
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Introduction

The following document contains an overview of the electrical and physical aspects of the Bug Module Interface (BMI) for users designing hardware for integration with the BugLabs platform. The focus is primarily on the requirements for compatibility with the BugBase 2.0. Be aware that there are several discrepancies between the interfaces found on the BugBase 2.0 and previous generations of the platform.

High Level System Overview

A functional block diagram of the Bug system architecture can be found in Drawing 1. The Bug platform consists of a BugBase as well as a range of modules. The BugBase is the core of the system and exposes a range of low level interfaces, such as USB, SPI, I2C, and UART through four BMI ports. Module housings are designed to interlock with the BugBase and can be 'snapped' on to expand the functionality of the system through these low level interfaces.



Drawing 1: Functional block diagram of BugBase 2.0.

Nomenclature

BMI (Bug Module Interface) – the electrical and physical interface between the Bug Base and modularized hardware that conforms to the PIM form-factor. Please note that this term is also used in the context of software.

PIM (Plug-In Module) – in the interest of eliminating confusion between modularized electronic components and modular Bug hardware, the term PIM refers to a modularized piece of hardware that conforms to the Bug form-factor and BMI specifications.

Base – system core; houses processor, memory, network interfaces, etc..

Slot – the port into which a PIM may be plugged. Each BugBase has four slots, though it is important to note that there may be significant as well as subtle differences between the functionality that a specific slot can accommodate. Slots may be classified as standard, video and battery. Additionally, differences exist between the standard slots found on BugBase 1.x and 2.0. Slot numbering on the schematics range from 1 to 4. In the software and in this document, however, slot numbers range from 0 to 3.

Standard Slot – slots with standard BMI functionality; non-Video slots. On BugBase 2.0 slots 0 and 2 are standard slots and slot 3 is compatible with a standard slot.

Battery Slot – slots that accommodate additional battery and/or power supply options for powering the Bug. These are identical to standard slots except that unused pins in the standard slot allow access to various power nodes on the BugBase. On BugBase 2.0, slot 3 is the battery slot. Additional information on the battery slot for BugBase 2.0 is provided in section Power Distribution and Options on page 12.

Video Slot – slots that accommodate only video related functionality. These slots feature a 24 bit parallel interface to OMAP's DSS (display subsystem). On BugBase 2.0 slot 1 is a video slot.

Slot Summary

Slot summary

BugBase 2.0	
Slot 0: Standard	Slot 1: Video
Slot 2: Standard	Slot 3: Standard, Battery

Electrical Design Considerations

Power

All standard PIM slots provide 5V on pins 2 and 39 of the BMI connector. Current drawn from each slot must not exceed 750mA. Section Power Distribution and Options on page 12 or the BugBase schematics can be consulted for additional details on how power is distributed to specific slots.

Interfaces

The following interfaces are made available on the PIM slots:

Bus	Signal Name	Dir	Description
Power – See section Power Distribution and Options on page 12.			The BugBase switches between two sources of power. One is the internal battery and the other is external power provided from the power jack. External power is used to power the bug and charge the battery when it is present. On the BugBase schematics, the switched internal power node is called VBAT. The final switch to VBAT is an ideal diode, which means that a higher voltage applied to VBAT “wins” and will safely supply power to the system.
	VBAT	P	VBAT is the power source node to the BugBase from which all other voltages are generated. It is the switched between the battery and external power. This net is exposed via the Battery Slot so that additional power sources can power the Bug. The ideal diode protects this net when external sources drive it such that higher voltage wins.
	VDD_5V	P	This is 5V generated from a switching power supply on the BugBase. It is derived from VBAT and can supply 750mA of current.
	VDD_CHRG_5V	P	This is connected to VBAT via a power switch (FDC6331L).
	LCD_VBAT	P	This is connected to VBAT via a power switch (FDC6331L).
	GND	P	Ground.
SPI - Serial Peripheral Interface.			The Serial Peripheral Interface Bus or SPI bus is a synchronous serial data link standard that operates in full duplex mode. The BugBase acts as master and PIMs communicate in slave mode. Because only a single chip select line (SPI_CSB) is exposed, only a single slave device can be easily used. Sometimes SPI is called a “four-wire” serial bus. All SPI signals are referenced to 3.3V.
	SPI_CLK	O	Serial Clock – BugBase generates this clock. Frequency is software programmable.
	SPI_CSB	O	Chip Select (active low)
	SPI_MOSI	O	Master Output, Slave Input
	SPI_MISO	I	Master Input, Slave Output
UART / RS-232 Serial			RS-232 (Recommended Standard 232) is the traditional name for a series of standards for serial binary single-ended data and control signals connecting between a DTE (Data Terminal Equipment) and a DCE (Data Circuit-terminating Equipment). In this case, the DTE is the BugBase and the DCE is the PIM. It is commonly used in computer serial ports. While the standard defines the electrical characteristics including voltage levels, these RS-232 signals are standard 3.3V CMOS signal levels. Thus a RS-232 UART Interface chip such as part number ICL3232IBN manufactured by Intersil would be required to talk with a standard RS-232 device such as a computer serial port. All UART signals are referenced to 3.3V.
	RXD	I	Received Data: Data from DCE to DTE.
	TXD	O	Transmitted Data: Data from DTE to DCE.
	RTS	O	Request to Send: DTE requests the DCE prepare to receive data.
	CTS	I	Clear to Send: Indicates the DCE is ready to accept data.

Bus	Signal Name	Dir	Description
I2C - Inter-Integrated Circuit			I2C is generically referred to as a "two-wire interface" and is a multi-master serial single-ended bus. SMBus, defined by Intel in 1995, is a subset of I ² C that defines the protocols more strictly. One purpose of SMBus is to promote robustness and interoperability. Accordingly, modern I2C systems incorporate policies and rules from SMBus, sometimes supporting both I2C and SMBus with minimal re-configuration required. Pullup resistors of 4.7K to 3.3V.
	SCL	I/O	Serial Clock.
	SDA	I/O	Serial Data.
USB			Universal Serial Bus 2.0. Compatible with high-speed, full-speed, and low-speed devices.
	USB_DP	I/O	Positive serial line.
	USB_DN	I/O	Negative serial line.
Interrupt	INT#	I	Active-low interrupt pin.
GPIO	GPIO[3:0]	I/O	General purpose Input/Output pins. Can be configured as inputs or outputs using the standard GPIO Linux kernel interface.
Camera			High speed camera interface. All three standard slots on the BugBase 2.0 share this interface, so scheduling must be handled in software.
	CAMERA_P	I	
	CAMERA_N	I	
McBSP – Multi-channel Buffered Serial Port			Each of the standard PIM interfaces exposes one of the McBSP's (Multi-channel Buffered Serial Ports) of the OMAP. The McBSPs are a full-duplex direct serial interface between the OMAP and other devices in the system such as audio and voice codecs and other application chips. See OMAP35x Technical Reference Manual from Texas Instruments web site for more information.
	BSP_DR	I	Receive serial data.
	BSP_DX	I/O	Transmit serial data.
	BSP_CLKX	I/O	Transmit clock.
	BSP_FSX	I/O	Transmit frame synchronization.
PIM Detection	PRESENT#	I	Connects directly to the OMAP processor and should be tied to ground on the PIM to signal to the OMAP when a PIM has been connected.

Table 1: Bug interface options. Pin direction are referred to the BugBase. I-input, O-output, P-power.

Pin Tolerance

All pins exposed by the BMI connector are buffered except for the presence pin (36). Please consult BugLabs or the BugBase schematics for more information regarding individual pin tolerances.

Typical PIM Hardware

Presence Pin

The presence pin on all BMI connectors must be grounded. This pin sends an interrupt to the BugBase processor to notify the system that a module has been inserted or removed.

EEPROM

All modules are required to have an I2C EEPROM with an I2C address configured to 0x50. The EEPROM must contain the modules PIM ID and vendor ID. Following the detection of a plug event (presence pin interrupt) the BMI software infrastructure will interrogate this EEPROM to identify which module has been plugged, and which driver

should be loaded. Please consult BugLabs to make the I2C EEPROM IC that you select is appropriate.

IO Expander

Because only four general purpose I/Os are available on the BMI connector, nearly all modules carry an IO expander on the I2C bus. This is not a requirement, but in many cases is necessary.

LEDs

Though not a strict requirement of BMI, nearly all modules carry a red/green bicolor LED. The red LED is typically controlled by GPIO3 and the green is typically controlled by GPIO2. These should be active low, and are typically placed in the lower left corner of the module when viewing the PIM from above with the BMI connector toward the bottom. The Dialight 598-8410-207F is an example bicolor LED used by BugLabs.

Table 2: Key physical design considerations.

Non-Standard Board Layouts

- Double Wide PIMs – for applications where the resources or area provided by a single BMI slot are insufficient, modules may be made to span two BMI slots. Please note that if a double wide PIM is designed to use two standard BMI slots, it will only fit on the bottom side of the BugBase 2.0 in slots 2 and 3.
- Stackable PIMs – To further enhance modularity, it is possible to stack PIMs by passing interface singles through a second female BMI connector mounted on the opposite side of the PIM. This can cause a great deal of complexity in software, so please consult BugLabs before beginning such a design.

Components on bottom side of PCB

If possible, designers should avoid placing parts on the rear side of the PIM PCBs. The standard PIM mating-side housing, however, does allow a clearance of 1.0mm outside of the specified component keepout region for low-profile components. A custom mating-side housing can be designed to adjust the keepout region and/or allow slightly more clearance in certain regions.

BMI Connector Layout

- All pre-2.0 PIMs and non-video PIMs: Chamfered keys on Samtec connectors toward the closest PCB edge.
- Add Video PIMs (2.0+): Chamfered keys on Samtec connectors away from closest PCB edge.

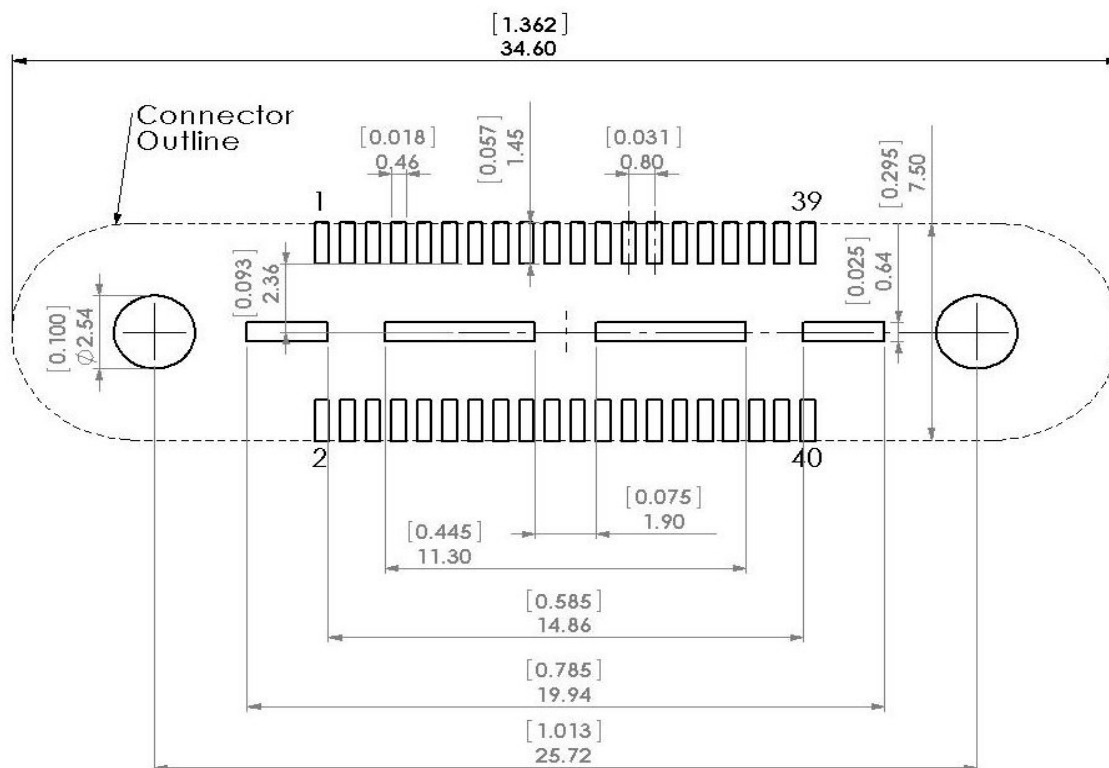
BMI Connectors

- Module-side connector (male) – the standard male BMI connector is a custom Samtec QTE series connector. Our custom Samtec part number is ASP-132124-01. To obtain this connector you may either contact BugLabs or Samtec directly. The connector is a standard QTE-020/QSE-020 mate. It is modified with two ears that allow the part to be secured to the PCB with fasteners. The recommended PCB footprint is shown in Drawing 3.
- Base-side connector (female) – the female BMI connector on the BugBase is a standard Samtec QSE-020 series connector. The specific Samtec part number is QSE-020-01-F-D-A-GP. To obtain this connector please contact Samtec directly. The manufacturer suggested land pattern for this part can be found on Samtec's webpage.

Additional Physical Considerations

- PIM Jacks/Ports – If a module requires edge-mounted ports (usb jacks/audio jacks/etc) it is best practice to place these on the PCB edge closest to or furthest from the BMI connector. This prevents the possibility of these jacks being inaccessible if the PIM is placed next to a second PIM when in use on the BugBase.
- Serial number location – A location for the serial number should be placed on the back side of every PCB. This location should be defined in the silkscreen by a rectangle 0.125" x 0.750".
- Bare board name and revision – The name and revision number of the PCB should be displayed in either the top or bottom copper/silk screen layer of each board.
- Fiducials – These features should be 0.030 round, should appear in three corners of the board, and should be at least 0.100" from the board edge.
- Logos – The BugLabs logo and if appropriate, the Open Hardware logo, should be displayed in silk screen on the board.

Mechanical Drawing and Pinout Table for PIM Modules



Drawing 3: Top view drawing of recommended PCB footprint for Samtec module-side connector. Units are in mm [inches].

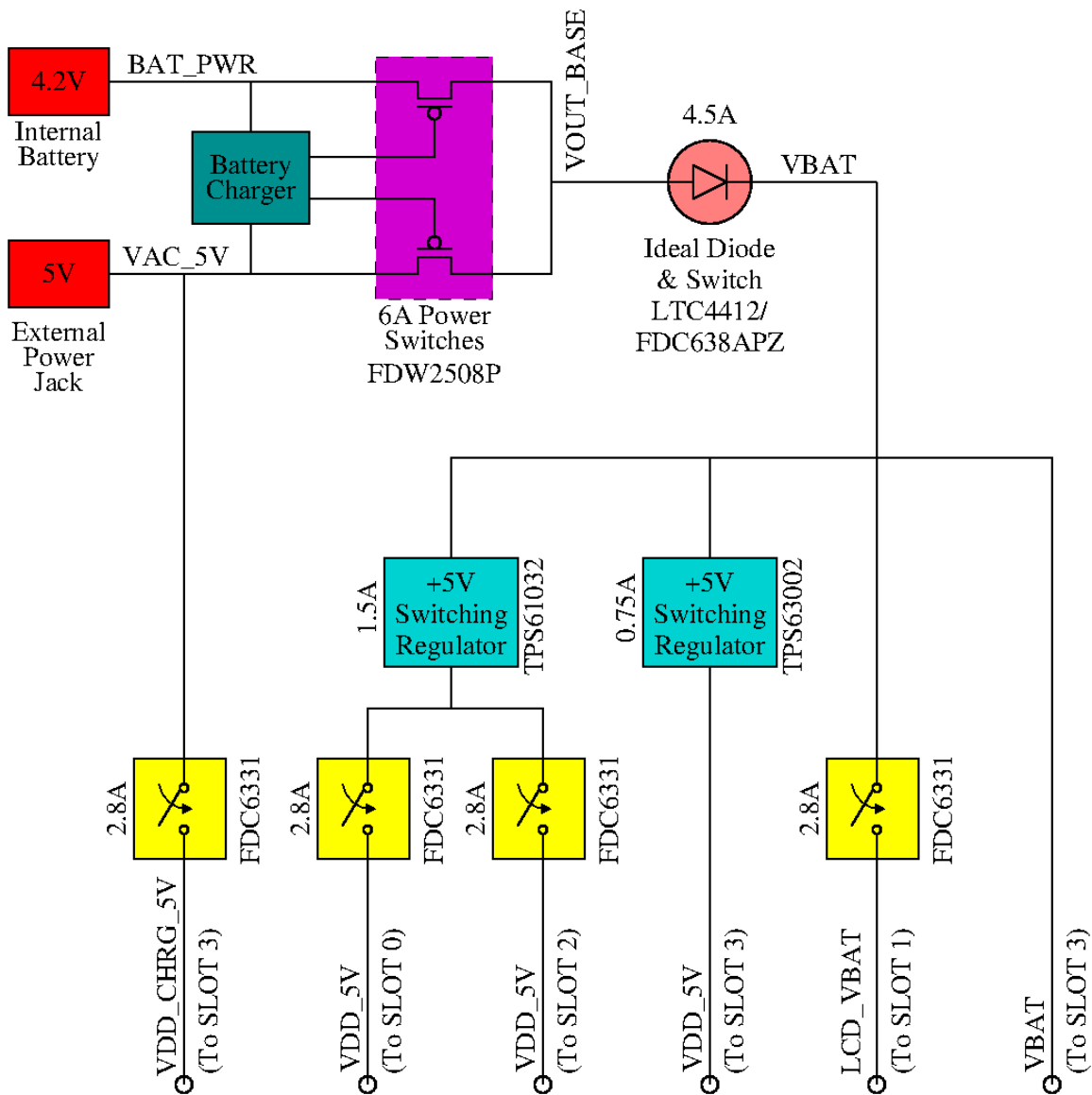
The following table provides pin assignments to the various interface signals available to each type of slot.

Pin Number	Standard Slot	Battery Slot	Video Slot
1		VBAT	LCD_D23
2	VDD_5V	VDD_5V	LCD_VBAT
3		VBAT	LCD_D22
4	SPI_MISO	SPI_MISO	LCD_D17
5	PRESENT#	PRESENT#	LCD_D21
6	SPI_MOSI	SPI_MOSI	LCD_D16
7		GND	LCD_D20
8	SPI_CSB	SPI_CSB	LCD_D15
9			LCD_D19
10	SPI_SCK	SPI_SCK	LCD_D14
11			LCD_D18
12			LCD_D13
13	GND	GND	LCD_VBAT
14	GND	GND	LCD_D12
15	UART_RXD	UART_RXD	LCD_PCLK
16	I2C_SCL	I2C_SCL	LCD_D11

Pin Number	Standard Slot	Battery Slot	Video Slot
17	UART_TXD	UART_TXD	LCD_HSYNC
18	I2C_SDA	I2C_SDA	LCD_D10
19	UART_CTS	UART_CTS	LCD_VSYNC
20	GPIO3	GPIO3	LCD_D9
21	UART_RTS	UART_RTS	I2C_SDA
22	INT#	INT#	LCD_D8
23	GPIO0	GPIO0	I2C_SCL
24	GPIO2	GPIO2	LCD_D7
25	BSP_CLKX	BSP_CLKX	LCD_DE
26			LCD_D6
27	BSP_FSX	BSP_FSX	LCD_VBAT
28	GPIO1	GPIO1	LCD_D5
29	BSP_DX	BSP_DX	TV_SVIDEO_C
30	GND	GND	LCD_D4
31	BSP_DR	BSP_DR	TV_SVIDEO_Y
32			LCD_D3
33	GND	GND	BL_PWM
34	GND	GND	LCD_D2
35	USB_DP	USB_DP	INT2#
36	CAMERA_P	CAMERA_P	PRESENT#
37	USB_DN	USB_DN	INT1#
38	CAMERA_N	CAMERA_N	LCD_D1
39	VDD_5V	VDD_5V	LCD_VBAT
40		VDD_CHRG_5V	LCD_D0

Power Distribution and Options

Power on the BugBase is distributed as shown in the simplified schematic in Drawing 4. Power comes from either an internal battery or external power jack. The internal battery has a nominal voltage between 4.2V and 3.2V. The external power jack supplies typically +5.3 to +5.0V. The battery charging chip detects when external power is applied and charges the battery as well as switches between the two supplies. Thus, when external power is present, the bug base system runs off the external power and the internal battery otherwise. The switched power supply is then conditioned further by an ideal diode and switching regulators to produce 5V levels sent to each of the standard slots. The Video Slot (Slot 1) and Battery Slot (Slot 3) get access to the raw system power (LCD_VBAT and VBAT).



Drawing 4: Simplified schematic of power distribution on BugBase.

Battery Slot

The Battery Slot is unique in that it is supplied the raw system power (VBAT) after being conditioned by an ideal diode. The ideal diode allows the battery module to safely and easily override and thus supply system power. The ideal diode will turn off whenever a higher voltage is detected and otherwise it will turn on. This means that the battery slot can either draw or supply system power depending on how it is configured. To supply power, it should provide a higher voltage. In the case of an external battery supplying power, it will safely draw power from both the internal battery and the external battery safely as power will be drawn from whichever is higher. A diode or ideal diode should be put in series on the battery slot to protect it as necessary whenever external power is connected to prevent damaging or over-charging an external battery. In that case, the battery module can access to the raw external power (VDD_CHRG_5V) so that it can charge any batteries it

may have. A maximum of 4.5A can be drawn from VBAT and 2.8A from VDD_CHRG_5V.

Standard Slots

Standard slots can draw up to 750 mA from the VDD_5V supply and should use this to generate a +3.3V reference for the various interface buses (e.g. I2C, SPI, etc).